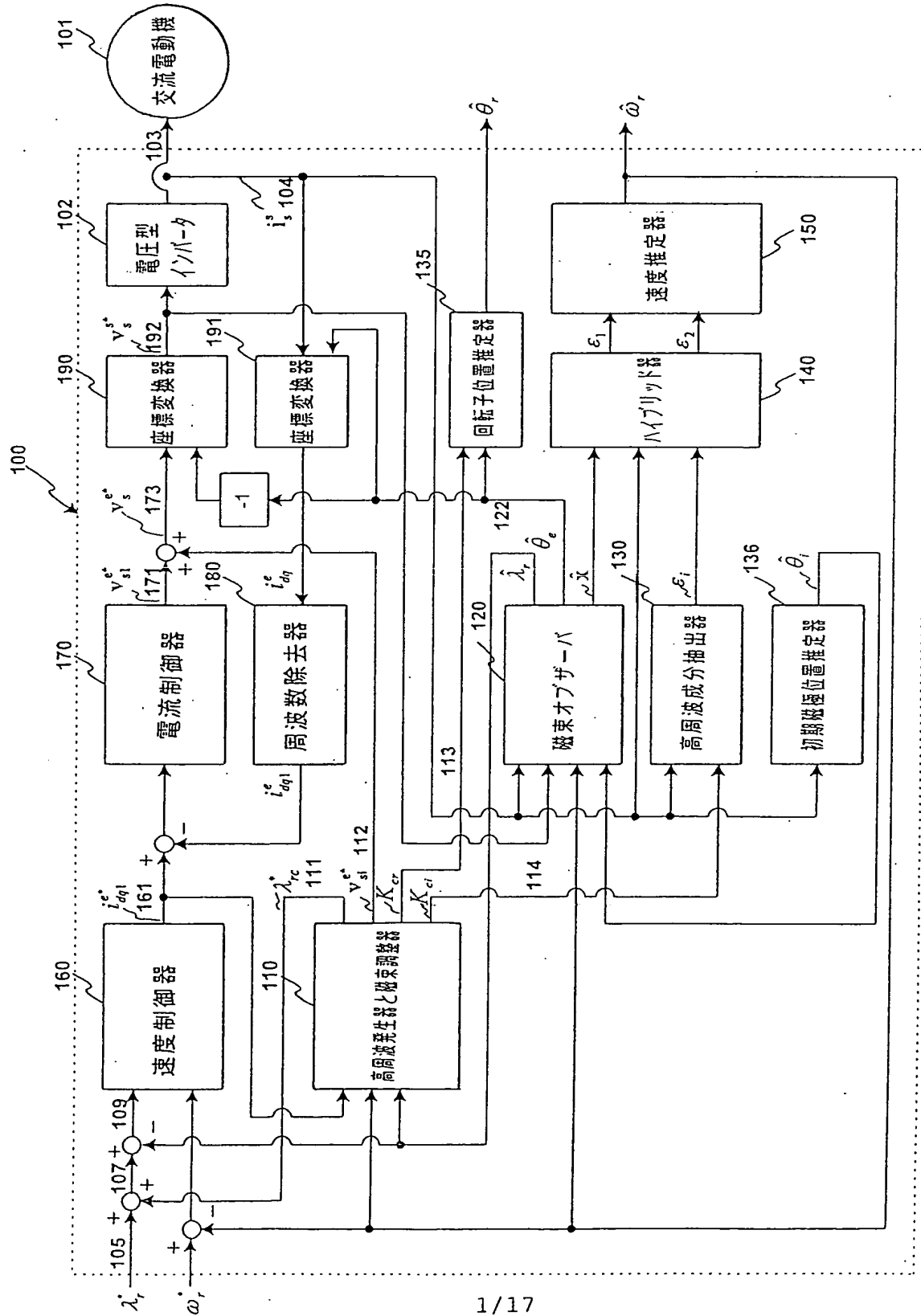


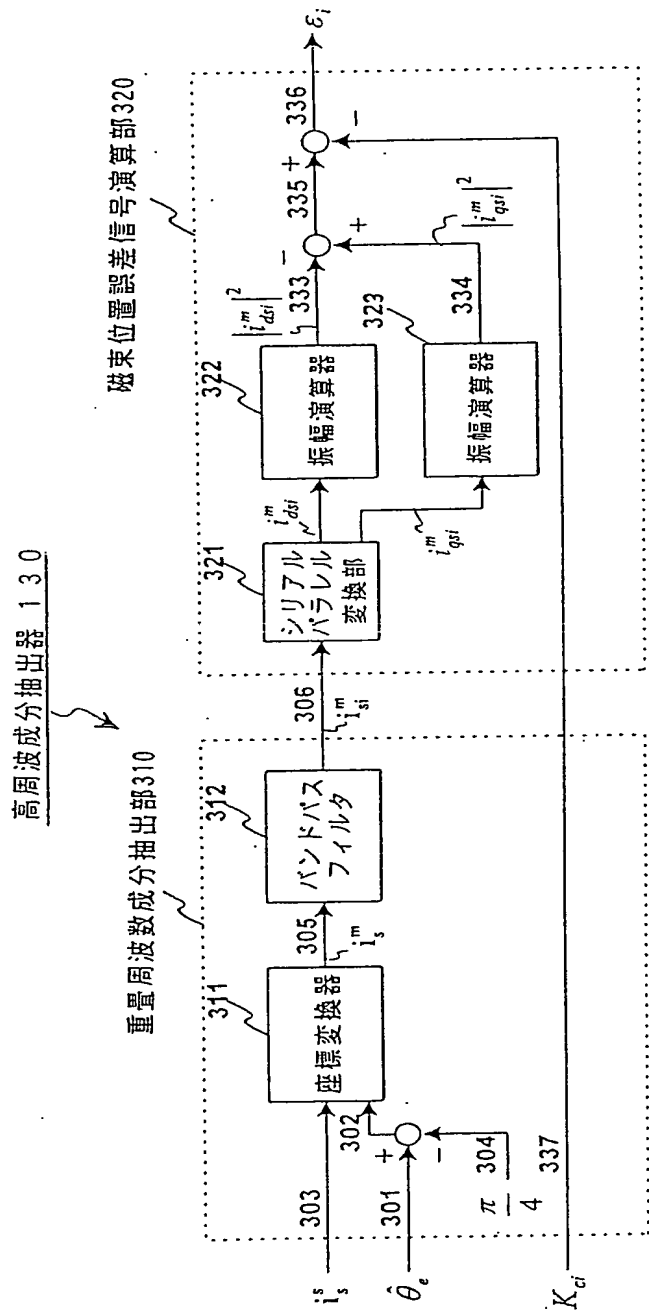
Fig. 1



The diagram illustrates a control system architecture, likely for a power converter, featuring several interconnected functional blocks:

- Block 210 (Control Logic):** This central block contains a summing junction (242) and a block labeled $1/s$ (242). It receives inputs from the reference current i_s^* (233) and the reference angular velocity $\hat{\omega}_r$ (235). It also receives feedback signals \hat{i}_s (225) and $\hat{\theta}_e$ (226). The output of the summing junction is fed into the $1/s$ block, which then feeds into block C (204).
- Block 220 (Prediction/Calculation):** This block contains a block labeled $C1$ (221) and two blocks labeled "预测量演算器" (Prediction Quantity Calculator), 223 and 224. Block 221 receives \hat{i}_s (225) and $\hat{\theta}_e$ (226) and outputs \hat{i}_s (227). Block 223 receives \hat{i}_s (227) and outputs \hat{i}_s (225). Block 224 receives $\hat{\theta}_e$ (227) and outputs $\hat{\theta}_e$ (226).
- Block 230 (Filtering):** This block contains two blocks labeled "信号衰减器" (Signal Attenuator), 211 and 212. Block 211 receives i_s^* (233) and outputs i_{dq1}^s (211). Block 212 receives $\hat{\omega}_r$ (235) and outputs $\hat{\omega}_{dq1}^s$ (212).
- Block 240 (Feedback/Control):** This block contains a block labeled N (240) and a block labeled A (202). Block N receives \hat{i}_s (225) and outputs i_s^* (233). Block A receives $\hat{\omega}_{dq1}^s$ (212) and outputs $\hat{\omega}_r$ (235).
- Other Blocks:** Block B (203) receives i_{dq1}^s (211) and outputs i_{dq1}^s (212). Block G (204) receives $\hat{\omega}_{dq1}^s$ (212) and outputs $\hat{\omega}_r$ (235). Block C (204) receives the output of the $1/s$ block and outputs \hat{i}_s (225).

Fig. 3

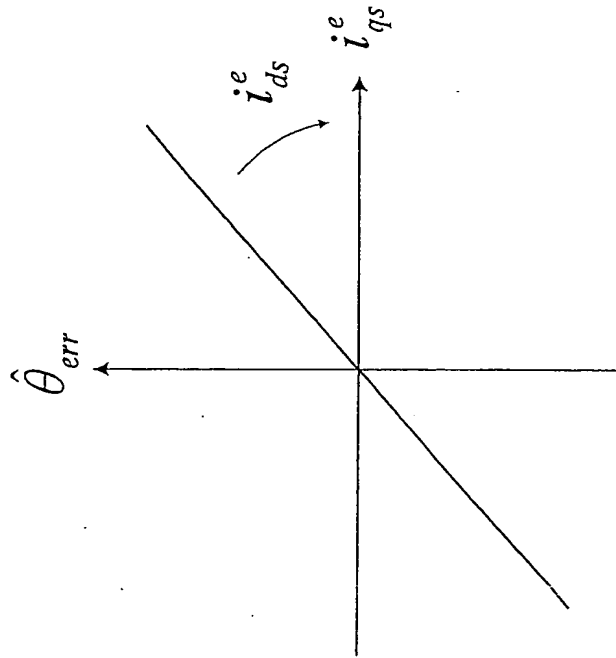


4/17

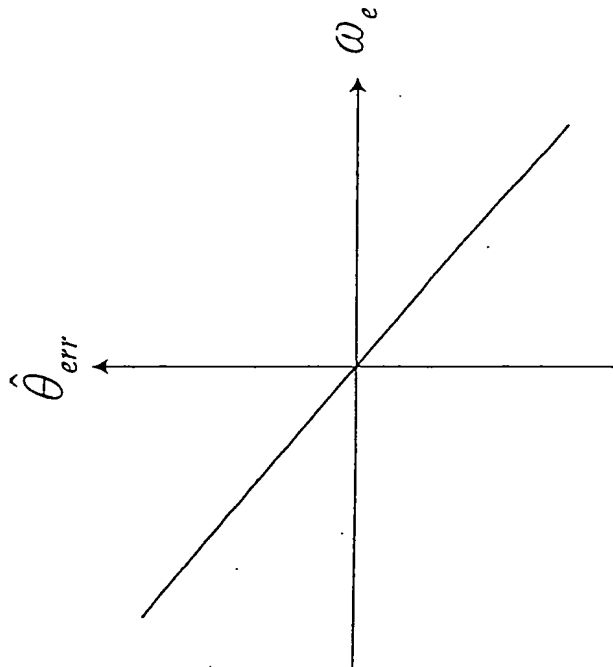
The diagram illustrates a control system for a motor, likely a brushless motor, with the following components and signal flow:

- Input Signals:**
 - $\hat{\omega}_r$ (540): Reference angular velocity.
 - i_{s1}^* (556): Reference stator current.
- Processing Blocks:**
 - 541:** A summing junction that calculates the error signal $\hat{\omega}_{cr1} = \hat{\omega}_r - \hat{\omega}_{cr}$.
 - Kc1:** A gain block that processes the error signal $\hat{\omega}_{cr1}$.
 - 545:** A summing junction that calculates the error signal $\hat{\omega}_{cr2} = \hat{\omega}_{cr1} - \hat{\omega}_{cr}$.
 - Kc2:** A gain block that processes the error signal $\hat{\omega}_{cr2}$.
 - Kc3:** A gain block that processes the error signal $\hat{\omega}_{cr2}$.
 - Kc4:** A gain block that processes the error signal $\hat{\omega}_{cr2}$.
 - Kc5:** A gain block that processes the error signal $\hat{\omega}_{cr2}$.
 - 546:** A summing junction that calculates the reference current $i_{ds}^* = \hat{\omega}_{cr2} + i_{ds}$.
 - 547:** A summing junction that calculates the reference current $i_{qs}^* = \hat{\omega}_{cr2} + i_{qs}$.
 - 550:** A block labeled "マップングテーブル" (Mapping Table) that receives $\hat{\omega}_{cr1}$ and outputs λ_{cr} (521).
 - 551:** A block labeled "マップングテーブル" (Mapping Table) that receives $\hat{\omega}_{cr1}$ and outputs v_{ds}^* (511).
 - 552:** A block labeled "マップングテーブル" (Mapping Table) that receives $\hat{\omega}_{cr1}$ and outputs v_{qs}^* (515).
 - 553:** A block labeled "マップングテーブル" (Mapping Table) that receives $\hat{\omega}_{cr1}$ and outputs K_{di} (531).
 - 554:** A block labeled "マップングテーブル" (Mapping Table) that receives $\hat{\omega}_{cr1}$ and outputs K_{ci} (561).
- Control Signals:**
 - i_{ds}^* (546) and i_{qs}^* (547) are the reference currents for the d-axis and q-axis, respectively.
 - v_{ds}^* (511) and v_{qs}^* (515) are the reference voltages for the d-axis and q-axis, respectively.
 - λ_{cr} (521) is the reference flux linkage.
 - K_{di} (531) and K_{ci} (561) are the current feedback gains for the d-axis and q-axis, respectively.

~~Fig. 7~~ Fig. 7



~~Fig. 6~~ Fig. 6



~~8~~ Fig. 8

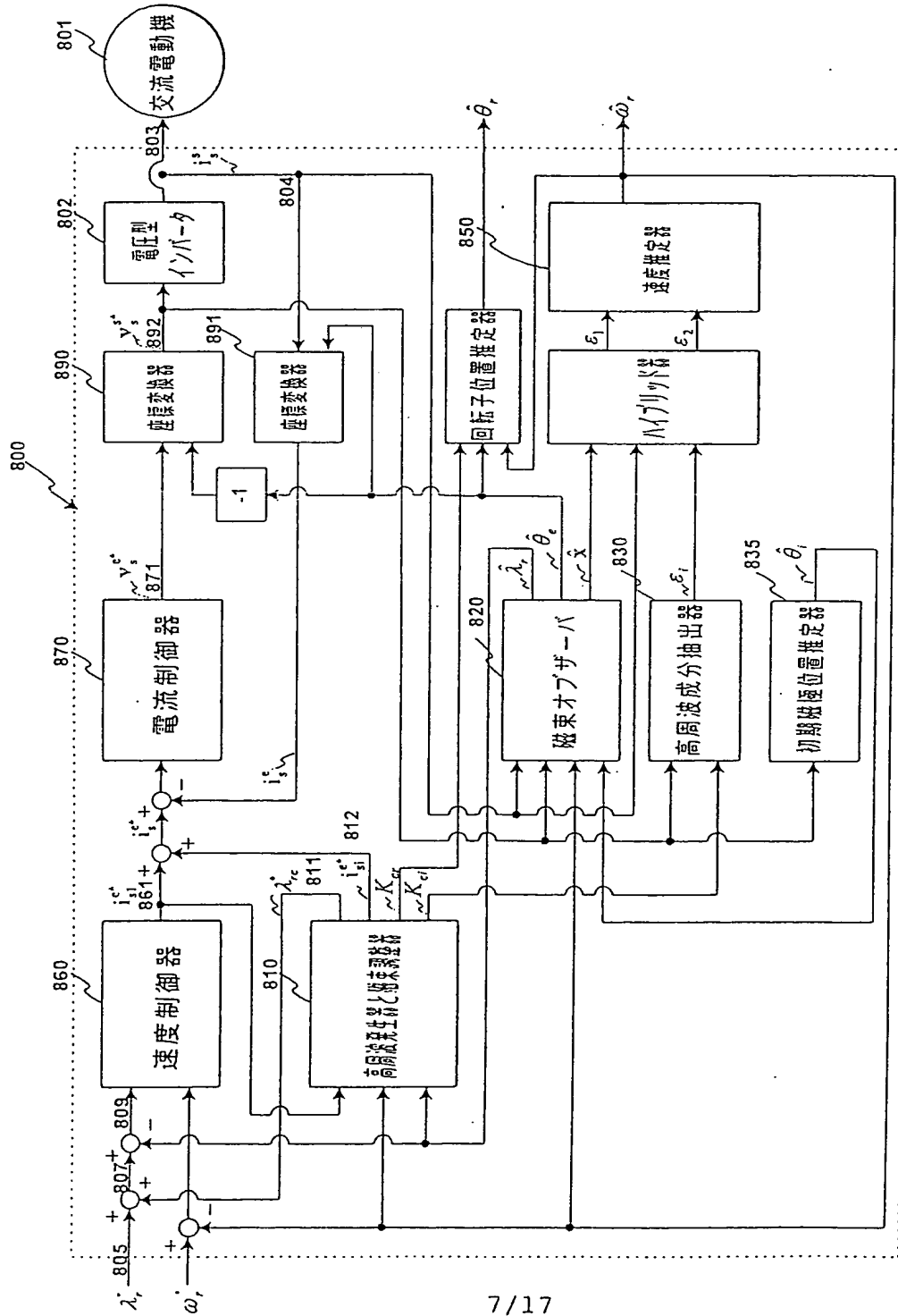
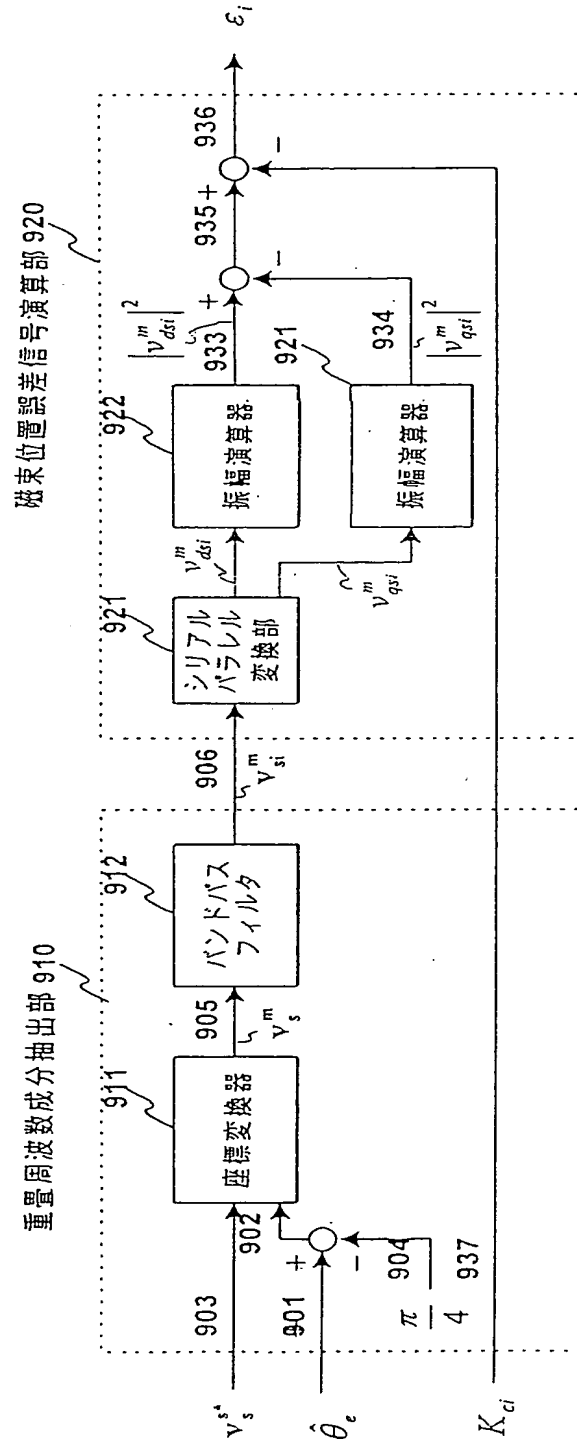
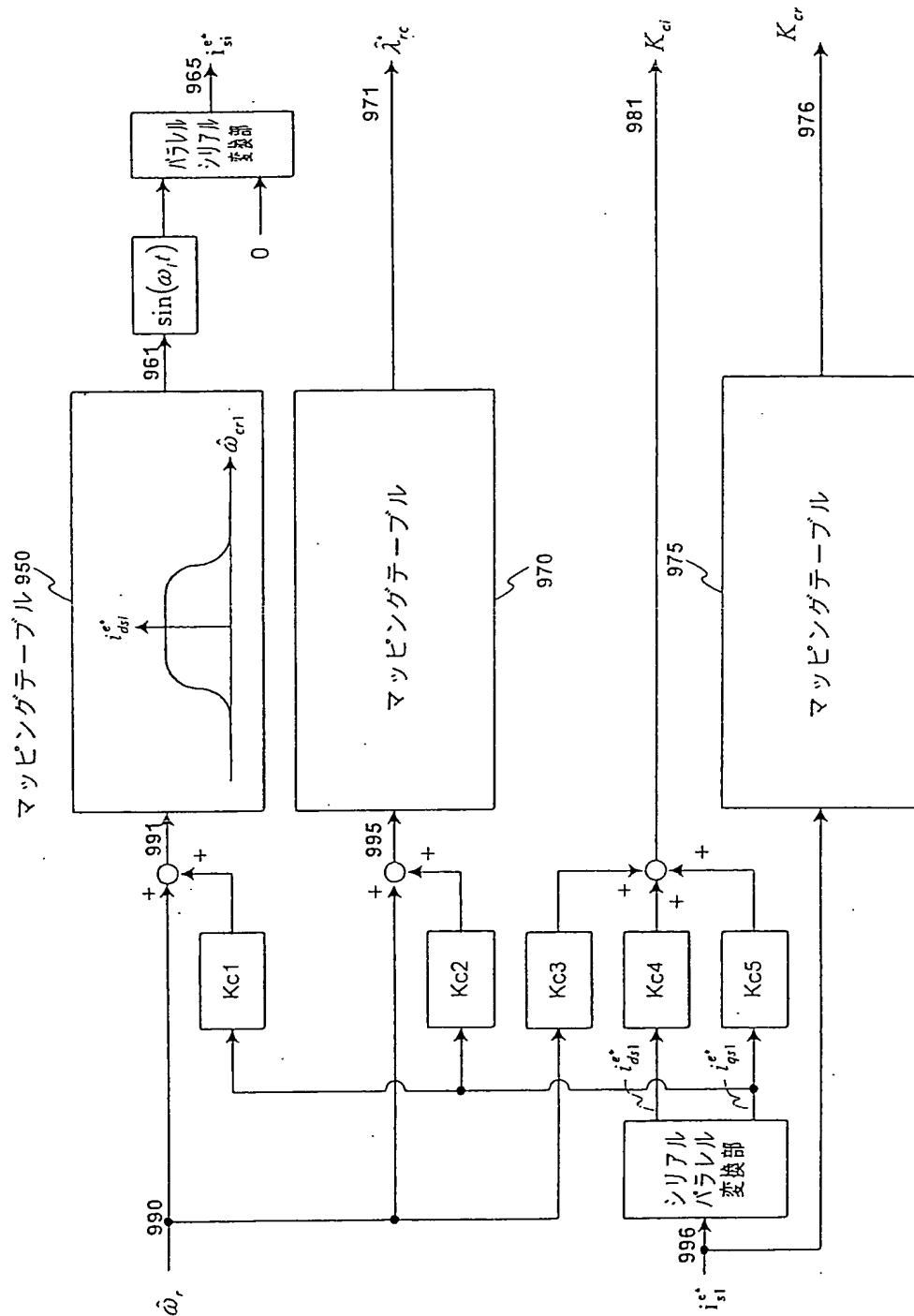


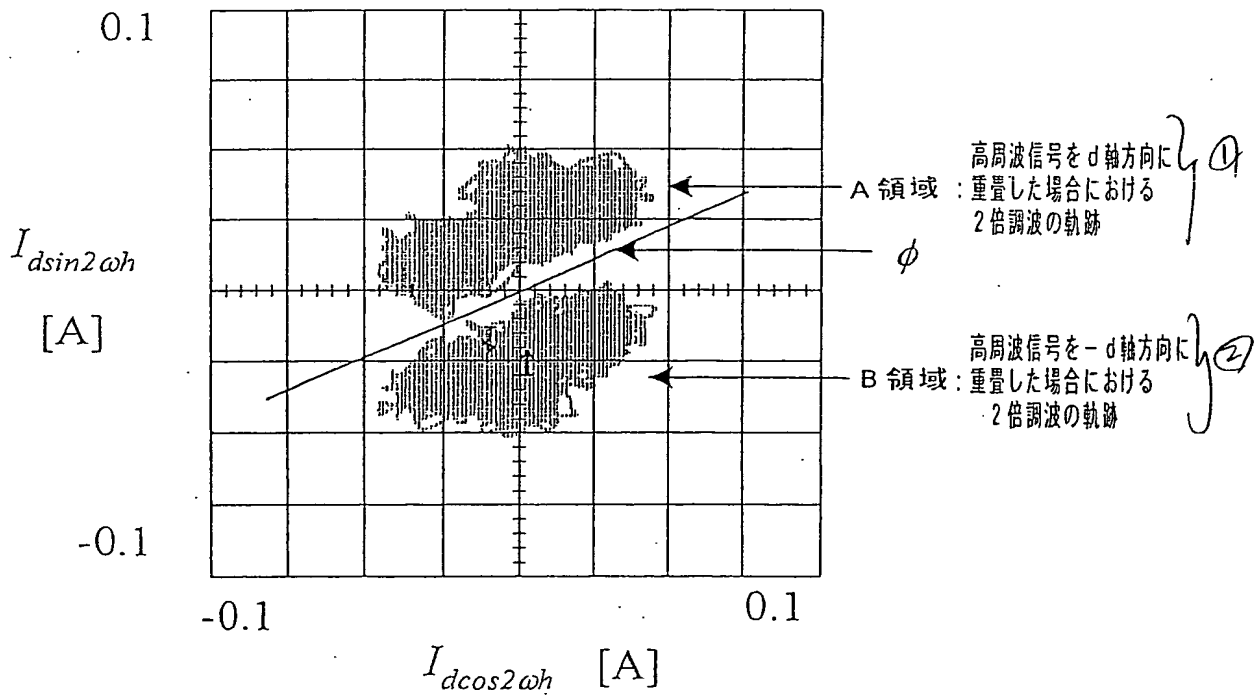
Fig. 9



~~Fig. 10~~ Fig. 10



~~Fig. 11~~ Fig. 11



BEST AVAILABLE COPY

~~Fig. 12~~ Fig. 12

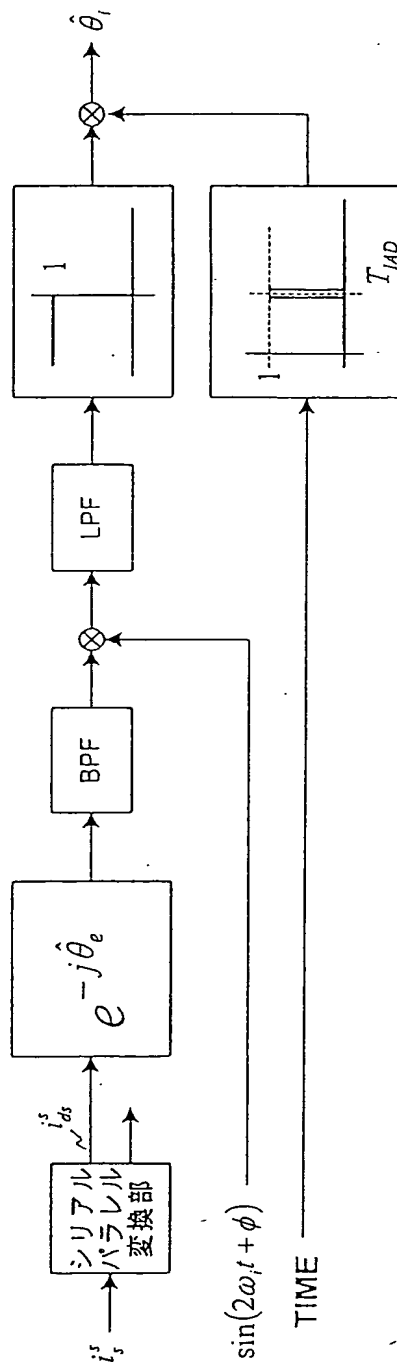


Fig. 13

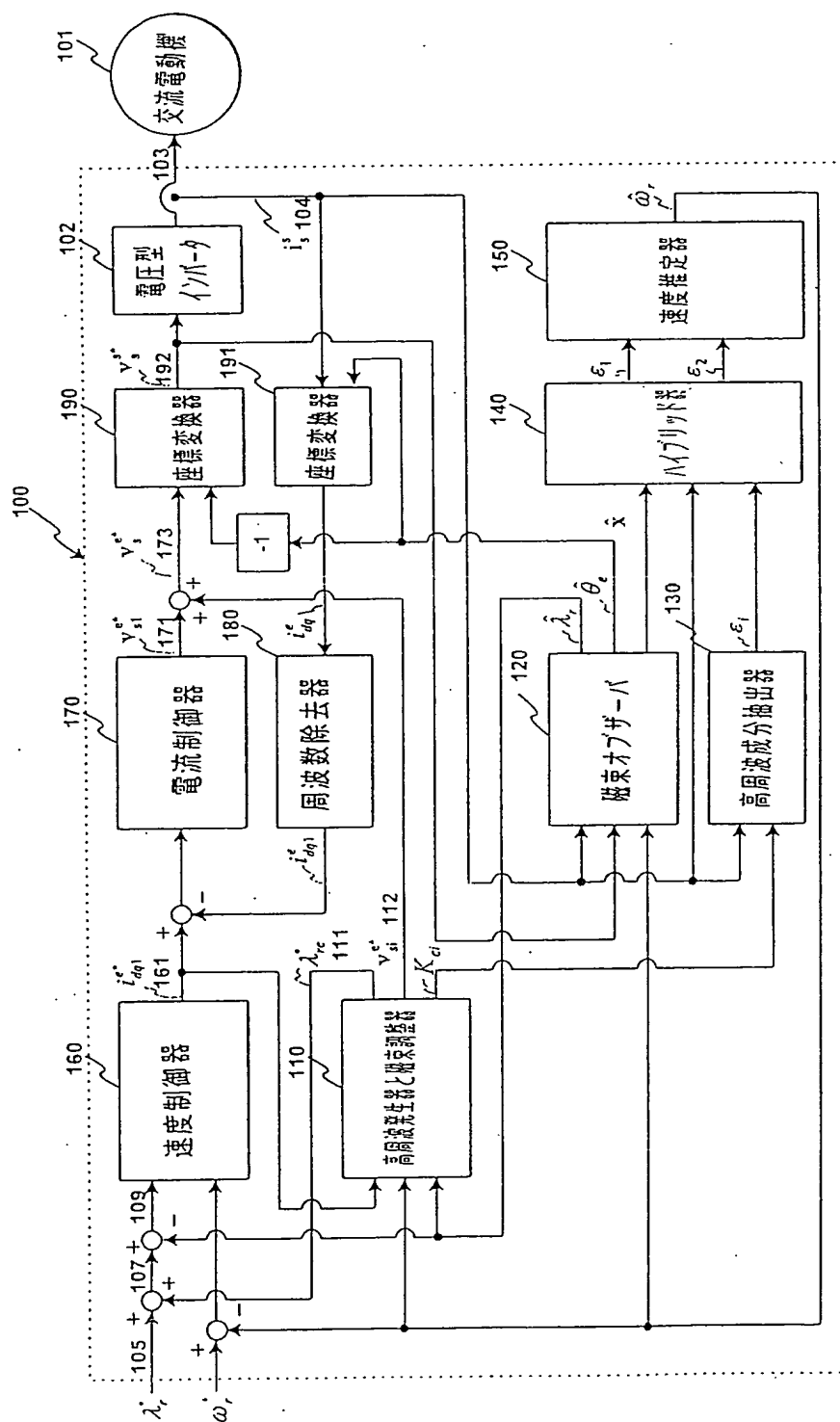


Fig. 14

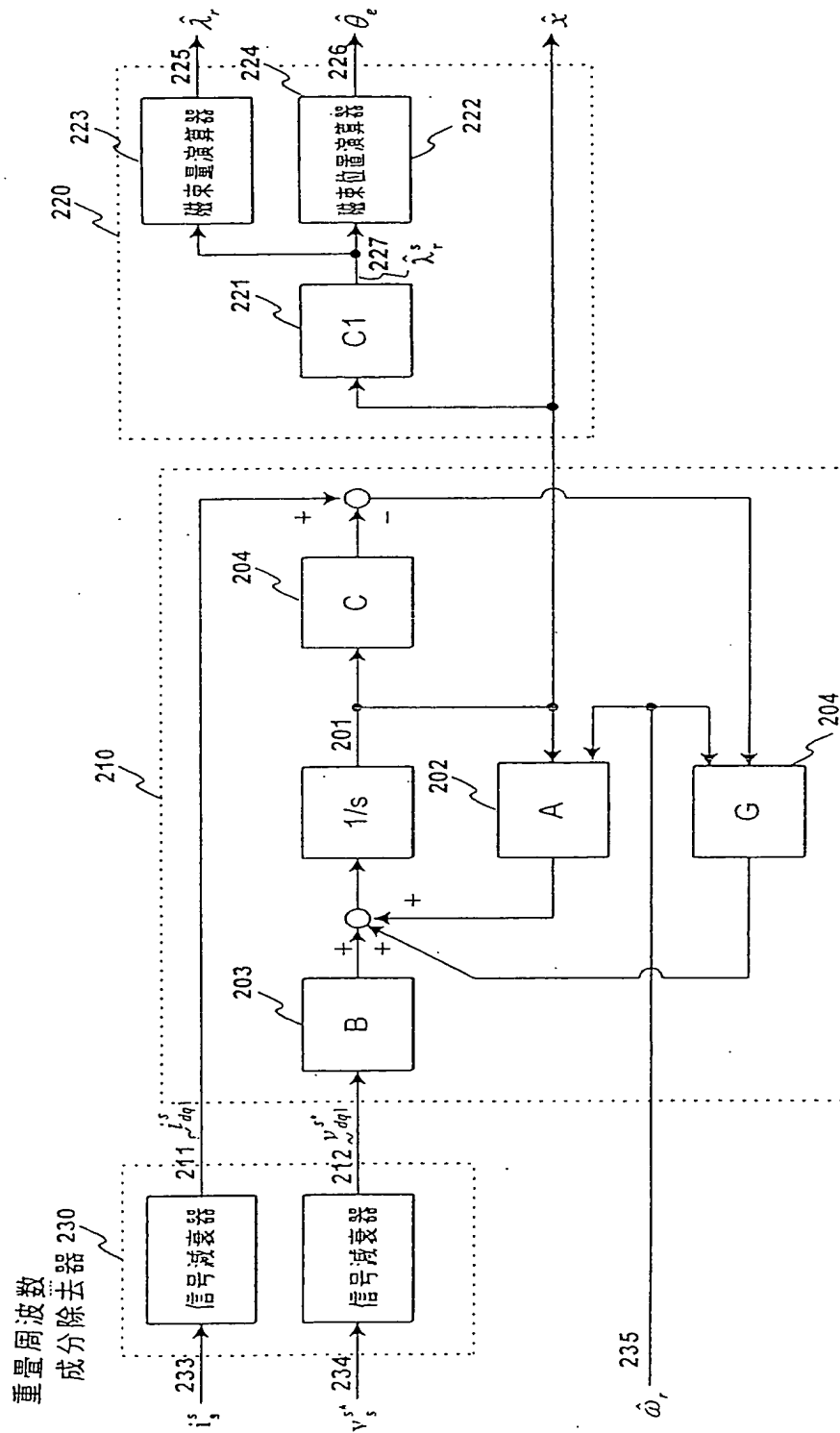


Fig. 15

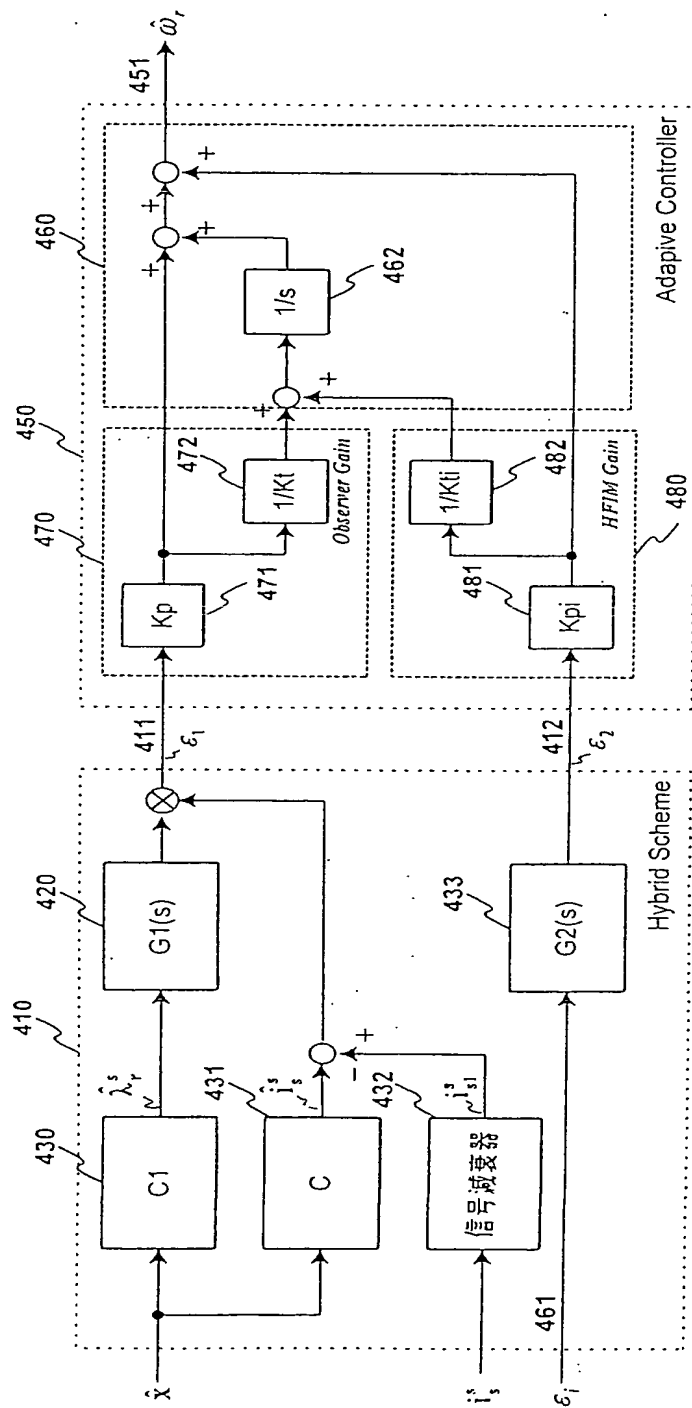


Fig. 16

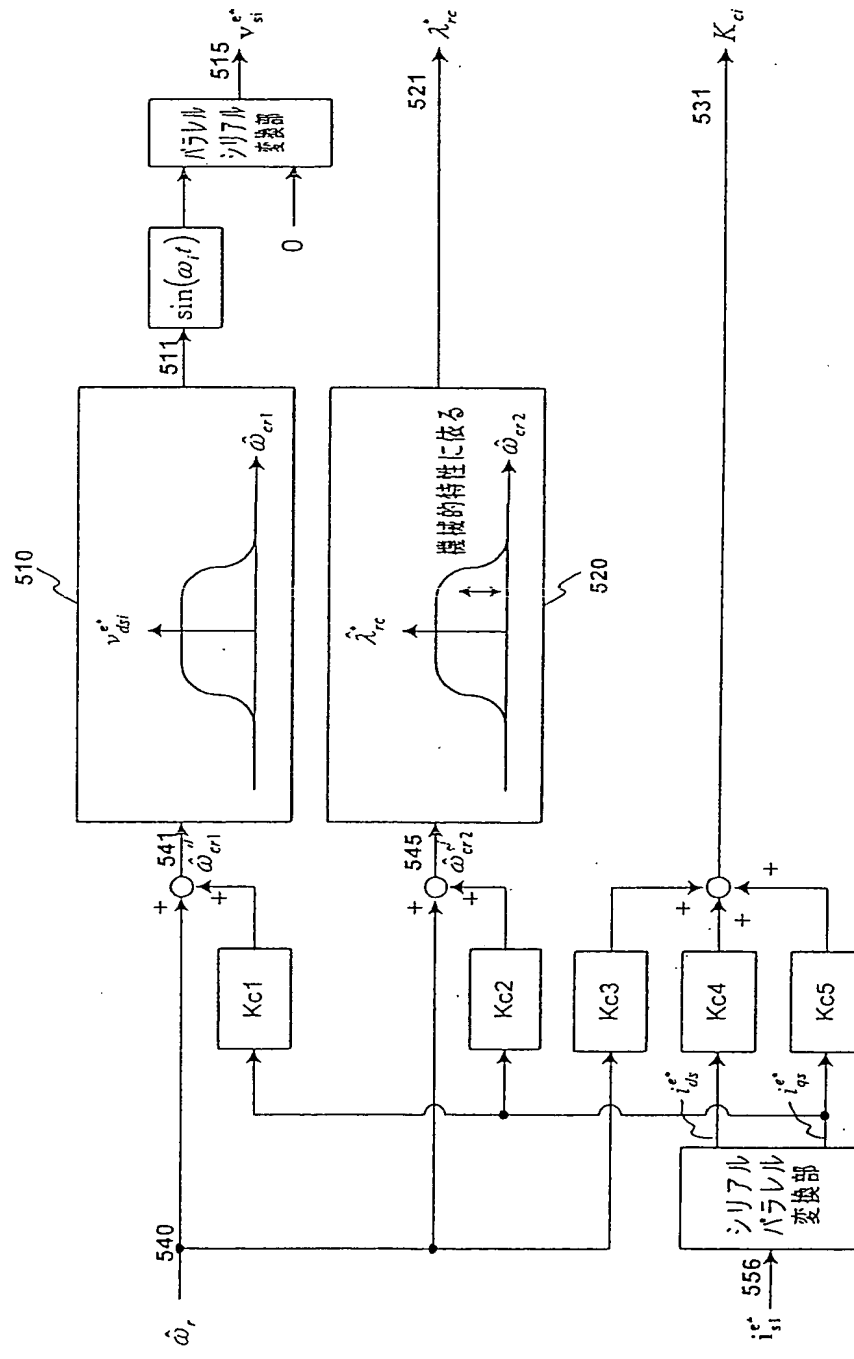


Fig. 17

